7 151. (Twice Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation comprises:

receiving an external clock signal;

receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code;

sampling the first operation code synchronously with respect to the external clock signal wherein the first operation code instructs the memory device to perform a read operation; and

outputting the amount of data in response to the first operation code.

2 152. (Twice Amended) The method of claim 1 151 wherein the block size information also defines an amount of data to be input by the memory device, wherein the amount of data is input in response to a second operation code, and wherein the second operation code instructs the memory device to perform a write operation, the method further including:

sampling the second operation code synchronously with respect to a transition of the external clock signal; and

inputting the amount of data in response to the second operation code.

6 156. (Twice Amended) The method of claim 1 151 wherein the memory device samples the block size information synchronously with respect to the external clock signal.

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~~161~~. (Twice Amended) The method of claim ~~151~~ wherein the block size information is an encoded value and wherein the block size information is sampled synchronously with respect to a rising or falling edge of the external clock signal.

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~~165~~. (Twice Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells, the method of controlling the memory device comprises:

issuing block size information to the memory device synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device; and

issuing a first operation code to the memory device synchronously with respect to the external clock signal, wherein the first operation code instructs the memory device to perform a read operation.

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~~176~~. (Twice Amended) A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code; and

a plurality of output drivers to output the amount of data in response to the first operation code.

179. (Twice Amended) The memory device of claim 176 wherein the input receiver circuitry samples the first operation code synchronously with respect to the external clock signal.